

EAST - [Untitled1:1]

File View Edit Tools Window Help

Active

- L1: (234273) (series or serial or cascade\$1) near5 parallel
- L2: (5666) (PE or PEs or processor\$ or (process\$3 or arithmetic or logic) adj (element\$1 or unit\$...
- L3: (59) \$2configur\$4 near5 2
- L4: (14) 3.ab.
- L5: (21) 3.clm. not 4
- L6: (24) 3 not (4 or 5)
- L7: (11) Backward citation search 1
- L8: (91) 708/524.ccls.
- L9: (158) 708/523.ccls.
- L10: (148) 9 not 8
- L11: (648) 708/490.ccls.
- L12: (630) 11 not (3 or 7 or 8 or 9)
- L13: (7) 2 and 12
- L14: (46801) input adj (mux or multiplex\$3 or select\$3)
- L15: (59694) output adj (mux or multiplex\$3 or select\$3)
- L16: (38) 12 and 14 and 15
- L17: (197) 712/15.ccls.
- L18: (5) Backward citation search 2
- L19: (30) Forward citation search 1
- L20: (16719) multiply adj add or multiply adj accumulat\$3 or mac
- L21: (69052) alu or arithmetic logic or adder
- L22: (629) 20 with 21
- L23: (11) 22 same 14
- L24: (216) 22 and 14
- L25: (93) 22 with parallel
- L26: (45) 14 and 25
- L27: (42) 26 not 11
- L28: (66) dyadic operation
- L29: (30) monadic operation
- L31: (0) trinomial operation
- L30: (19) 28 and 29
- L32: (120) 708/605.ccls.
- L33: (16798) (PE or PEs or processor\$ or (process\$3 or arithmetic or logic) adj (element\$1 or uni...
- L34: (729) \$2configur\$4 near5 33
- L35: (35) 34.ti.
- L36: (119) 34.ab.
- L37: (106) 36 not 35
- L38: (11) 37 and 14 and 15
- L39: (1) 37 and 14 not 20

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DBs US-PGPUB: USPAT: USOCR: EPO: JP Plurals

Default operator: ADJ Highlight all hit terms initially

BRS form S&R form Image Text HTML

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- ☒ L27: (42) 26 not 11
- ☒ L28: (66) dyadic operation
- ☒ L29: (30) monadic operation
- ☒ L31: (0) trinomial operation
- ☒ L30: (19) 28 and 29
- ☒ L32: (120) 708/605.ccls.
- ☒ L33: (16798) (PE or PEs or processor\$ or (process\$3 or arithmetic or logic) adj (element\$1 or uni...
- ☒ L34: (729) \$2configur\$4 near5 33
- ☒ L35: (35) 34.li.
- ☒ L36: (119) 34.ab.
- ☒ L37: (106) 36 not 35
- ☒ L38: (11) 37 and 14 and 15
- ☒ L39: (1) 37 and 14 not 38
- ☒ L40: (71) 34 and 14 same 15
- ☒ L41: (62) 40 not (35 or 38)
- ☒ L42: (1010) 712/10-19.ccls.
- ☒ L43: (134) 42 and 14 and 15
- ☒ L44: (52) multiplier and 43
- ☒ L45: (82) 43 not 44

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DBs US-PGPUB:USPAT:USOCR:EPO:JP ☐ PluralsDefault operator: ADJ ☒ Highlight all hit terms initiallyBRS form  S&R form  Image  Text  HTML

	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re	Inventor
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6836839 B2	20041228	32	Adaptive integrated circuitry with heterogeneous and reconfigurable matrices of diverse and adaptive computational units having fixed application specific	712/29	710/312; 710/315		Master, Paul L. et
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6754805 B1	20040622	21	Method and apparatus for configurable multi-cell digital signal processing employing global parallel configuration	712/35	708/300; 708/422		Juan; Yujen
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6571268 B1	20030527	39	Multiplier accumulator circuits	708/524			Giacalone; Jean-P et al.
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6317770 B1	20011113	20	High speed digital signal processor	708/524	708/404; 708/523		Lim; Il Taek et al.
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6266760 B1	20010724	39	Intermediate-grain reconfigurable processing device	712/15	712/11		DeHon; Andre et a
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6247036 B1	20010612	47	Processor with reconfigurable arithmetic data path	708/603			Landers; George e
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6122719 A	20000919	33	Method and apparatus for retiming in a network of multiple context processing elements	712/15	709/220; 712/111		Mirsky; Ethan et al
8	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5852729 A	19981222	16	Code segment replacement apparatus and real time signal processor using same	712/225	704/258; 710/260		Limberis; Alexandre et al.
9	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5422805 A	19950606	9	Method and apparatus for multiplying two numbers using signed arithmetic	708/625	708/525; 708/530		McIntyre; Kenneth al.
10	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US RE34850 E	19950207	12	Digital signal processor	712/33	712/35; 712/43		Murakami; Tokumi al.
11	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5278781 A	19940111	10	Digital signal processing system	708/523	708/402		Aono; Kunitoshi et
12	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5241492 A	19930831	13	Apparatus for performing multiply and accumulate instructions with reduced power and a method therefor	708/523			Girardeau, Jr.; Jar W.